Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1. (**currently amended**) A substrate to be mounted with a semiconductor chip, comprising:

a plurality of insulation layers forming a laminated structure, said laminated structure having a chip-mounted surface in which a semiconductor chip is mounted; and

a built-in capacitor formed in said laminated structure, said built-in capacitor being integrated with said laminated structure **and being formed on a layer of organic polysilane in said substrate**, said built-in capacitor comprising:

a dielectric film; and

a pair of electrode layers sandwiching said dielectric film.

2. (original) The substrate as claimed in claim 1, wherein said insulation layer forming said chip-mounting surface is formed of a baked organic polysilane layer.

3. (original) The substrate as claimed in claim 2, wherein said baked organic polysilane layer comprises a baked polymethylphenyl silane layer.

4. (original) The substrate as claimed in claim 2, wherein said baked organic polysilane layer has a silicon skeleton and an organic substituent at a said chain of said skeleton.

5. (original) The substrate as claimed in claim 2, wherein said baked organic polysilane layer has a thermal expansion coefficient of about 2.6ppm/K at said mounting surface.

6. (original) The substrate as claimed in claim 2, wherein said baked organic polysilane layer has a Young modulus of about 1.2GPa.

7. (original) The substrate as claimed in claim 2, wherein said baked organic polysilane layer has a dielectric loss tangent of about 0.005.

8. (original) The substrate as claimed in claim 2, wherein said baked organic polysilane is baked at a temperature of 230°C or higher.

9. (original) The substrate as claimed in claim 1, wherein said substrate includes power feeding conductor and a ground conductor, and wherein said built-in capacitor is provided in electrical connection between said ground conductor and said power feeding conductor.

10. (original) The substrate as claimed in claim 9, wherein each of said power feeding conductor and said ground conductor extends continuously from a bottom surface of said substrate to a top surface of said substrate along a via-hole.

11. (original) The substrate as claimed in claim 10, wherein each of said power feeding conductor and said ground conductor has a projecting part projecting from said chip-mounting surface.

12. (original) The substrates as claimed in claim 11, wherein said projecting part extends laterally beyond a diameter of said via-hole along said chip-mounting substrate.

13. (original) The substrate as claimed in claim 11, wherein said projecting part has a rounded shape and extends laterally beyond a diameter of said via-hole in intimate contact with said chip-mounting surface.

14. (original) The substrate as claimed in claim 1, wherein said capacitor is formed between a first insulation layer and a second insulation layer formed on said first insulation layer in intimate contact with both of said first and second insulation layers, said first and second insulation layers being included in said plural insulation layers, one of said first and second insulation layers providing a said chip-mounting surface and being formed of a baked organic polysilane layer.

15. (original) A substrate to be mounted with a semiconductor chip, comprising:

a plurality of insulation layers forming a laminated structure, said laminated structure having a chip-mounted surface on which a semiconductor chip is mounted; and

first and second built-in capacitors each formed in said laminated structure at a first side and a second side of an insulation layer formed of a baked organic polysilane layer, each of said first and second built-in capacitors being integrated with said laminated structure,

each of said first and second built-in capacitors comprising a dielectric film and a pair of electrode layers sandwiching said dielectric film,

said first and second built-in capacitors being connected parallel with each other between a power feed path and a ground path extending continuously through said substrate from a bottom surface thereof to a top surface thereof.

16. (withdrawn) A method of manufacturing a substrate to be mounted with a semiconductor chip, said substrate comprising plurality of insulation layers forming a laminated structure and a capacitor provided in said laminated structure,

said method comprising the steps of:

forming said laminated structure by laminating said insulation films consecutively, said insulation films including a first insulation film and a second insulation film formed on said first insulation film,

wherein there are provided the steps, after forming said first insulation layer but before forming said second insulation layer, of: forming a first electride

film, forming a dielectric film on said first electrode film; and forming a second electrode film on said dielectric film.

17. (withdrawn) The method as claimed in claim 16, wherein said step of forming said laminated structure comprises the steps of:

forming a layer of organic polysilane;

pre-baking said layer of organic polysilane;

forming a via-hole in said organic polysilane; and

post-baking said layer of organic polysilane such that said layer of organic polysilane is converted to a baked organic polysilane layer,

said step of post-baking being conducted at a temperature of 230°C or higher.

18. (withdrawn) The method as claimed in claim 17, wherein said step of post-baking is conducted at a temperature of 500°C or higher.

19. (withdrawn) The method as claimed in claim 17, wherein said step of pre-baking is conducted at a temperature of about 120°C.

20. (withdrawn) The method as claimed in claim 16, wherein said step of forming said dielectric film comprises an anodization process of said first electrode film.